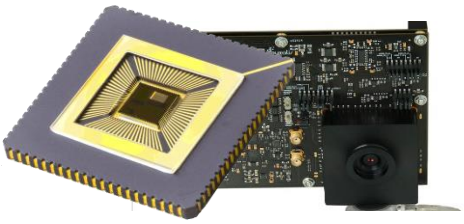
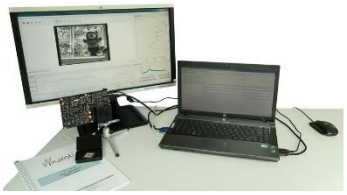
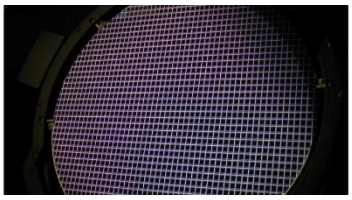
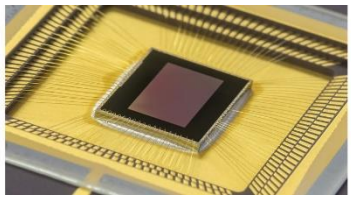
CREAPYX

Pixel Evaluation and Demonstration Platform

Fast and Flexible to the Pixel

pyxalis
Your Image Sensor Solution

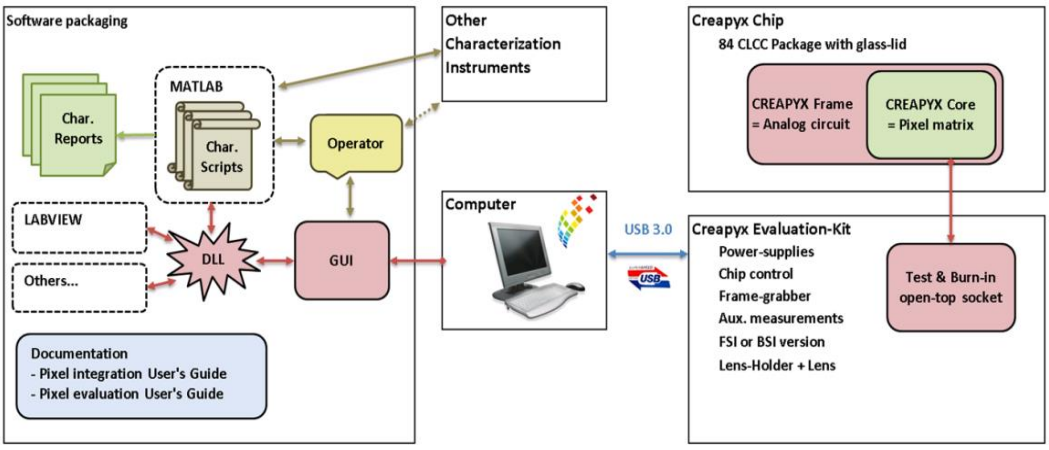
The CREAPYX is a unique, fast and flexible platform for new pixels evaluation.
It allows shortening the time to market for a new design as much as possible in order to focus on what matters: make the best pixel possible and test it as fast as possible.
The test system is delivered with a customized, fully silicon proven Pixel-frame layout, to the required dimensions, in the targeted technology (ST Microelectronic / Tower Jazz / LFoundry …)

Very Flexible approach:

- Up to 8 control signals per pixel line
- Rising and falling edge slew rate control
- Up to 3 level voltage applied on signal control lines
- Large range of power supplies
- Timing adjustment through IHM /EK
- Column bandwidth adjustment
- Column current control
- Matrix power supply dynamic control
- XY addressing through column control
- Test unit to visualize pixel signal control
- Available on multiple CIS process
- FSI or BSI

Compliant with:

- Different pixel sizes (< 1µm up to > 500µm)
- Different architectures (3T, 4T, 5T …)
- Shared architectures
- Ultra low noise pixel measurement
- Backside illumination
- High resistivity substrate
- Negative voltage on pixel control line
- Large range of power supply inputs
- HDR pixel with multiple readout
- Non-destructive readout
- Post process options
- CCD (charge transfer) concept
- Mechanical shutters and/or flash lights
- Bulk biasing
- TDI operation
- NMOS/PMOS pixel type
- 3V3 & 5V option



Creapyx facts sheet:

- 45+ successful Tape-out
- 400+ pixels variants evaluated
- 3 foundries
- 5 CMOS processes validated.

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CREAPYX Chip

Maximum resolution : VGA format

The chip package is a 84 lead ceramic LCC, sealed with a epoxy glued glass lid (Can be removed through heating)

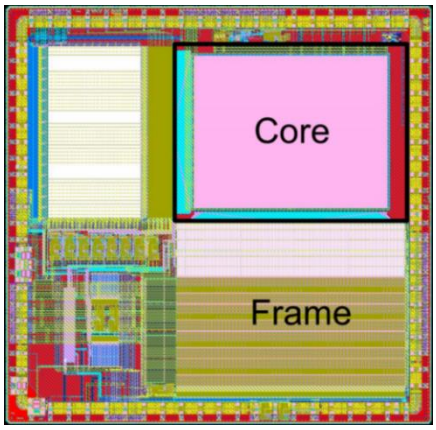
The total die size is 6,0 mm (V) x 5,9 mm (H) , compatible with standard MPW site.

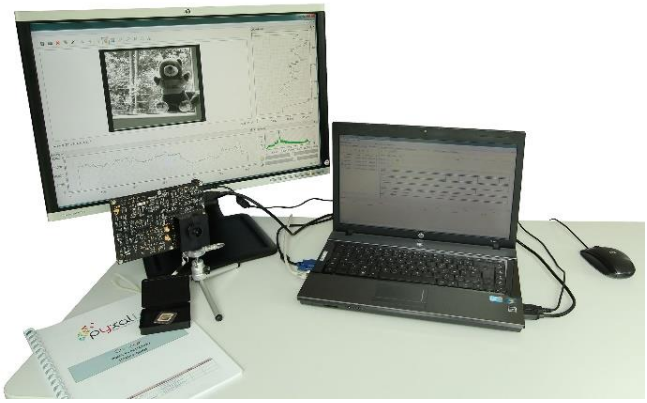
Design and layout is made out of :

- Core (Pixel array and interconnections)
- Frame (Needed driving and readout circuitry)
- Core has a total available area of 3,3 mm (H) x 2,5 mm (V)
- Pixel array area
- Interconnections to frame (for pitch fitting)
- Frame can be black-boxed for LVS purposes (abstract view to be used)

Delivery comprises :

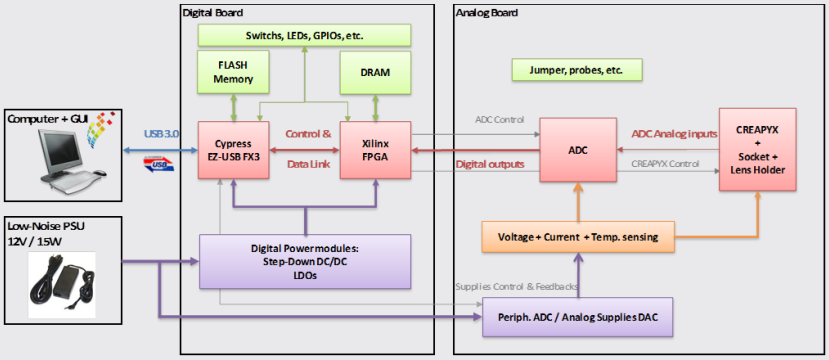
- Frame layout view
- Frame symbol view
- Frame empty schematic view (only pins)
- Frame abstract view
- Pixel integration user's guide
- Pixel integration in the frame takes only a few hours





Evaluation Kit

Usage of a Cypress FX3 MCU and Xilinx Artix7 FPGA
USB3 for frame-grabbing and EK control
FX3 handles CREAPYX register interface,
power supplies and data-link
FPGA handles frame and line sequencing
Dedicated low-noise supplies / analog inputs
Jumper and probes for observability / external supply
Auxiliary voltage/current measurements



Delivery comprises:

- Evaluation kit (packaged)
  - Digital and FSI analog boards (fully assembled and tested)
  - Optional BSI analog board
  - Optical mount with basic lens, tripod
  - Power supply, USB cable
- Software (digital download)
  - Graphical User interface with interface DLL (Maltlab, Labview…)
  - Optional characterization scripts for automation (Matlab only)
- Pixel evaluation user's guide

Evaluation kit is compliant with Creapyx chip in different processes

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