

HDPYX 130

1.3MP, 132dB, Flicker aware,
CMOS image sensor



The HDPYX-130 Sensor is a high performance, high dynamic range 1.3 MP image sensor. Designed for automotive, security and other demanding outdoor applications, the device offers supreme high dynamic range and numerous safety integrity features. An advanced synchronization facility allows stereo and multi-camera systems to work synchronously, minimizing system latency and motion temporal mismatch artifacts.

Key Features

Advanced HDR with 3 integration times and on-chip reconstruction for up to 22 bits output.

Embedded Piece Wise Linear (PWL) compression curve to convert the 22 bits HDR in 12bits output.

Set of motion and flicker minimizing HDR options. Flicker flag to indicate where flickering has been detected within a frame.

Advanced Dark calibration which estimates and subtracts dark current for each pixel and exposure.

Defective Pixel correction to correct dynamically single or duet defective pixels in Mono and Raw Bayer.

Windowing, image cropping and subsampling.

MIPI CSI-2 (2 Lanes / 55Mbps)

Parallel 12bits video interface (66Mp/s)

I2C (400MHz or 1GHz) fast control interface

Dual integrated temperature sensors.

Safety features.

Model

HDPYX 130

• Resolution Class	1.3 Megapixel
• Active Pixels	1304 x 980
• Aspect Ratio	4 : 3
• Frame Rate	45 fps
• Optical Diagonal	1/2.7"

Pixel Performance

- 3,75 μ m pitch
- Dynamic range up to 132 dB
- Linear Dynamic range up to 72 dB
- Pixel sensitivity $\geq 32V/lux.sec$ @3200K (no color filters)
- Peak SNR 42dB @ 12 lux
- Minimum illumination: 1 mlux (30ms integration, 5000K no filter)
- QE >60% @520nm
- Temporal noise < 0,025% @ full swing
- Image lag < 0.1% at 10ke- of signal

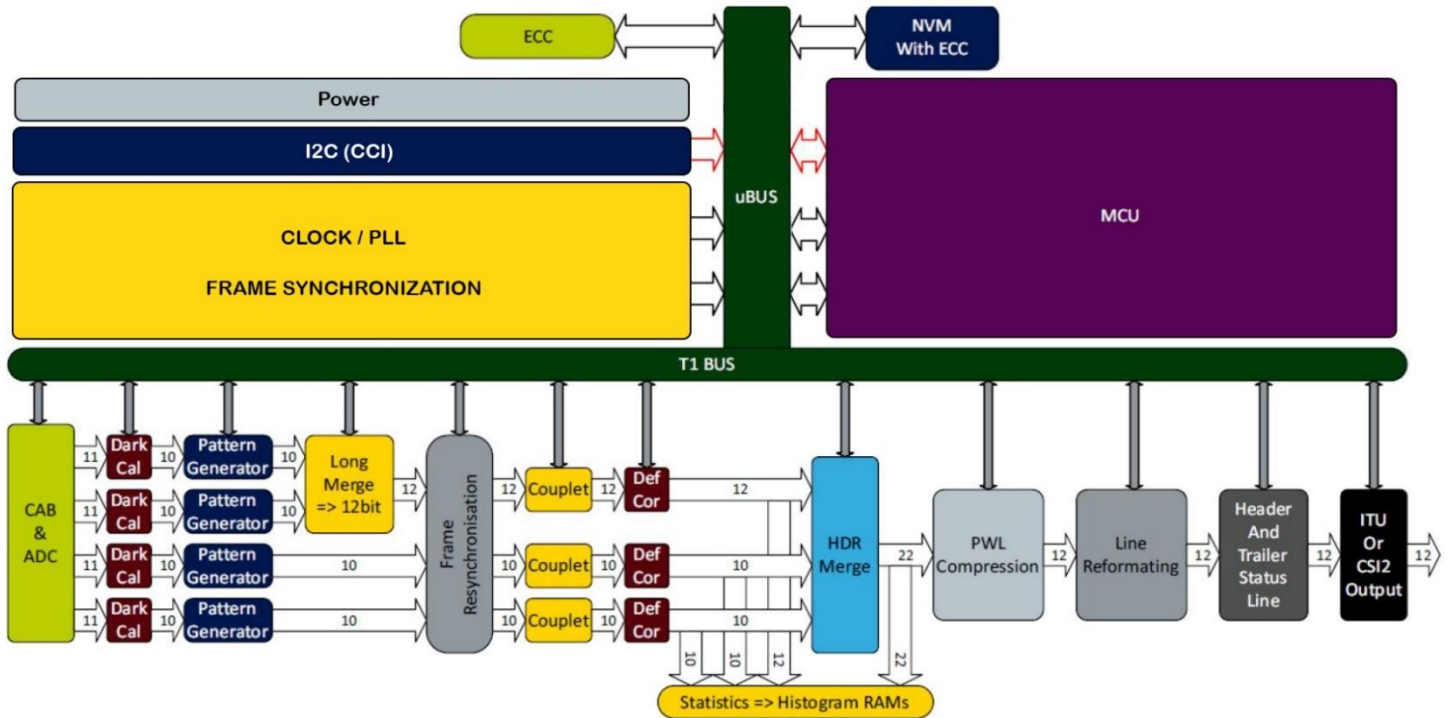
Environment

- Low power (400mW at Full Speed)
- Operating temperature of -40°C to 125°C
- Automotive qualified IM2BG4 plastic package
- Automotive qualification AEC-Q100 grade 2
- ASIL B Compliant
- BGA or bare die available



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Operation modes

The sensor can work in Linear mode with up to 10 bits per pixels
 HDR image capture is done in three phases:
 A Long exposure 12 bits (composed of 2 different Gain values).
 A medium and a short exposure in 10bits.
 The 3 exposures are merged in the HDR block with configurable algorithm providing a 22bits value which is compressed in 12bits in the embedded Piece Wise Linear (PWL) compression block.

ISP Special features

The HDR merge block includes ghost and Motion/ Light flickering removal possibilities.

The embedded PWL compression algorithm implements a 32 segments piecewise linear transfer function fully configurable to convert the 22bits HDR in 12bits output.

